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TITLE: CLOCK SYNCHRONIZATION APPARATUS AND METHOD OF DEVICES WITH DIFFERENT CLOCKS

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CLOCK SYNCHRONIZATION APPARATUS AND METHOD OF DEVICES WITH DIFFERENT CLOCKS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[1] The present invention relates to a clock synchronization of devices with different clocks and, more particularly, to an apparatus and method for synchronizing two devices with different operation clocks (referred to as 'clock', hereinafter).

2. Background of the Related Art

[2] In general, when a clock ratio between a RAM (e.g.., an SDRAM (Synchronous Dynamic Random Access Memory)) and a memory controller of a microprocessor is a ratio of 2:1, a clock speed of the RAM is regulated to slow down to have the same speed as the clock speed of the microprocessor. This helps synchronize the clock ratio to 1:1 in spite of an interface between the synchronous devices.

[3] If the clocks of each device to be interfaced do not agree with each other, the clock of a device with a fast clock speed must be lowered down to the level of the clock of a device with a slow clock speed for the purpose of interfacing. Therefore, the related art method for synchronizing the clock between two devices having a different clock has a problem that a maximum performance of the device with a fast clock speed is degraded as much as the clock speed is lowered.

SUMMARY OF THE INVENTION

[4] One exemplary embodiment of the present invention is to provide a clock-synchronizing apparatus and method of devices with different clocks that are capable of minimizing performance degradation of a device with a fast clock speed in case of interfacing devices each with a different clock speed.

[5] In another embodiment of the present invention, a clock-synchronizing apparatus and method of devices is provided with different clock that are capable of reducing an access latency that a device with a slow clock speed accesses a device with a fast clock speed, and capable of effectively using a transmission band width between two devices.

[6] In another embodiment of the present invention, a clock-synchronizing apparatus of devices with different clocks includes: a first device operated according to a first clock and generating control signals at the speed of a second clock; a second device operated by being synchronized with the second clock according to the control signals and having an operation latency of one clock period of the first clock; and a clock driver for generating the second clock by multiplying the first clock by certain even times and removing a phase delay between the second clock and the first clock.

[7] In another embodiment of the present invention, there is further provided a clock-synchronizing method of devices with different clocks including the steps of: programming a generation interval of RAM control signals so as to correspond to the operation latency of the RAM, for interfacing between a RAM with a speed of even times a clock speed of a microprocessor and the microprocessor; generating the RAM control signals corresponding to a specific operation mode at a RAM clock speed according to the

programmed generation interval and outputting it from the microprocessor to the RAM; and performing an operation according to the operation mode between the microprocessor and the RAM on the basis of the microprocessor clock by the RAM control signals generated at the RAM clock speed while maintaining the programmed generation interval.

[8] In another embodiment of the present invention, a clock-synchronizing apparatus of devices with different clocks includes a first device operated according to a first clock and generating control signals at a speed of a second clock; a second device operated by being synchronized with the second clock according to the control signals and having an operation latency of one clock period of the first clock; and a clock driver generating the second clock by multiplying the first clock by predetermined even times and removing a phase delay between the second clock and the first clock.

[9] In another embodiment, a clock-synchronizing method of devices with different clocks includes programming a generation interval of memory control signals so as to correspond to an operation latency of a memory interfacing between a microprocessor and the memory which has a speed of predetermined even times a speed of a microprocessor clock; generating the memory control signals corresponding to a specific operation mode at a speed of a memory clock according to the programmed generation interval and outputting the memory control signals from the microprocessor to the memory; and performing an operation according to the operation mode between the microprocessor and the memory on the basis of the microprocessor clock by the memory control signals generated at the speed of the memory clock according to the programmed generation interval.

[10] Additional advantages, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[11] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[12] Figure 1 illustrates an exemplary configuration of a clock-synchronizing apparatus of devices with different clocks in accordance with a preferred embodiment of the present invention;

[13] Figure 2 illustrates an exemplary method of generating RAM control signals at a RAM clock speed by a microprocessor;

[14] Figure 3 illustrates an exemplary timing diagram explaining a read operation of the microprocessor according to a clock suspension function of a RAM;

[15] Figure 4 illustrates an exemplary timing diagram explaining a write operation of the microprocessor according to a clock suspension function of a RAM;

[16] Figure 5 illustrates an exemplary timing diagram showing a clock-synchronizing method for a read operation of the microprocessor in accordance with another embodiment of the present invention;

[17] Figure 6 illustrates an exemplary timing diagram showing a clock-synchronizing method for a burst write operation of the microprocessor in accordance with still another embodiment of the present invention; and

[18] Figure 7 is a table showing comparison results between a performance of the related art interfacing method and that of an interfacing method of one embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[19] Figure 1 illustrates a configuration of a clock-synchronizing apparatus of devices with different clocks in accordance with a preferred embodiment of the present invention. Figure 1 depicts a clock-synchronizing apparatus of devices having different clocks including: a microprocessor 10 operated according to a 50 MHz clock and generating a RAM control signal according to a double clock of 50 MHz; a clock driver 30 for doubling the 50 MHz clock to generate a 100 MHz clock and compensating for a phase difference due to a propagation delay between the 50 MHz clock and the 100 MHz clock; and a RAM 20 operated according to the 100 MHz clock and for using two clock periods of the 100 MHz clock as an operation latency. Here, the two clock periods of the 100 MHz clock represent two ticks of the 100 MHz clock.

[20] The microprocessor 10 includes a memory controller (not shown in Figure 1) where the RAM control signal generation method can be programmed by a user. The memory controller can be a UPM (user programmable machine). A CKE (clock enable) pin of the RAM 20 is generally used in a pull up state but, in one embodiment of the present invention, it is connected to a GPL (general purpose line) port of the microprocessor 10. Accordingly, the RAM 20 has a clock suspension function of maintaining one more clock period of operation timing under the control of the microprocessor 10.

[21] Figure 2 shows a method of generating a RAM control signal according to double clock of 50 MHz, RAM clock, by the memory controller of the microprocessor 10. The microprocessor 10 obtains double clock of a 50 MHz clock by using a 1/4 period shifted clock of a system clock (50 MHz clock) and the system clock, and generates a RAM

control signal (RAM word) according to the obtained double clock of 50 MHz clock. Even if the microprocessor 10 is operated according to 50 MHz, the RAM control signal can be generated according to the 100 MHz clock by the memory controller of the microprocessor 10.

[22] Figure 3 illustrates an exemplary timing diagram explaining a read operation of the microprocessor according to a clock suspension function of the RAM. The following embodiment of the present invention presents an exemplary case where one clock period of the clock of the microprocessor 10 corresponds to two clock periods of the clock of the RAM 20. If the RAM 20 maintains a data outputting for as long as one clock period, a first output data of the RAM 20 can be recognized by the microprocessor 10. However, in the case of a burst read, a second data recognized by the microprocessor 10 will correspond to the third data of the RAM 20, and at the point when the microprocessor 10 recognizes third and fourth data, since the RAM 20 shall have already outputted all the data, the microprocessor 10 would fail to recognize a data.

[23] In addition, the RAM 20 expects a precharge after completing data outputting, whereas the microprocessor 10 expects a data recognition, so that the microprocessor 10 would lose the data stored in the RAM 20. In order to solve such problems, a clock suspension function of the RAM 20 is used.

[24] When the microprocessor 10 outputs a clock enable signal (CKE) to the RAM 20, an internal CKE signal of the RAM 20 suspends for 1 clock according to the clock enable signal CKE, according to which the RAM maintains a data outputting by as long as one more clock. Therefore, the RAM 20 can output a data for every one clock period of the

microprocessor 10 and the microprocessor 10 can read outputted data at every one clock period of the microprocessor 10. Therefore, the microprocessor 10 can read all the data outputted from the RAM 20 without a loss.

[25] Figure 4 illustrates an exemplary timing diagram explaining a write operation of the microprocessor according to the clock suspension function of a RAM. In case that the microprocessor burst-writes to the RAM 20, even though the microprocessor 10 outputs a data at every clock, those data are not inputted to the RAM 20 at every clock. A clock suspension function of the RAM 20 is used to address this issue.

[26] When the microprocessor 10 outputs a clock enable signal CKE to the RAM 20, an internal CKE signal of the RAM 20 suspends for one clock period according to the clock enable signal CKE, according to which the RAM 20 waits for data inputting for one clock period and then receives a data from the microprocessor 10 at a rising edge of the next clock period.

[27] Therefore, even though the microprocessor 10 outputs data at every two clock periods of the RAM 20, the RAM 20 can receive the data from the microprocessor 10 at every two clock periods. The microprocessor 10 practically outputs a data to a 'don't care' region. But since the RAM 20 does not care about the 'don't care' region, it does not matter.

[28] A clock-synchronizing method of devices with different clocks in accordance with another embodiment of the present invention will now be described. First, a generation interval of RAM control signals is programmed corresponding to an operation latency of the RAM 20 by a user. Next, in case of a specific operation mode between the microprocessor and the RAM, the microprocessor 10 outputs RAM control signals

corresponding to the specific operation mode to the RAM 20 and the microprocessor 10 and the RAM 20 interwork in the specific operation mode on the basis of a microprocessor clock (50 MHz). Thus, the RAM 20 and the microprocessor 10 can perform the specific operation mode on the basis of the microprocessor clock even though they are operated by using their own clock.

[29] Figure 5 illustrates an exemplary timing diagram showing a clock-synchronizing method for a read operation of the microprocessor in accordance with another embodiment of the present invention.

[30] First, the user programs the memory controller so that a desired RAM control signal can be generated from the memory controller of the microprocessor 10, which will now be described.

[31] In the case where the RAM 20 performs a data outputting operation, if the RAM 20 has two clock periods of the 100MHz clock as an operation latency from the clock driver 30, an RCD (RAS to CAS Delay), a CL (CAS Latency) and an RP (Precharge time) of the RAM 20 are respectively two clock periods and equivalent to one clock period of the microprocessor 10.

[32] The user programs RAM control signals as follows. The programming is done such that the RCD of the RAM 20 stored in a memory control table (UPM table) of the microprocessor 10 corresponds to one clock period of the microprocessor 10. The user programs a corresponding RAM control signal so that an RAS/ signal of the RAM 20 can be maintained in a low output state, that is, a state that the RAS/ signal is enabled only for a 1/4 clock of the microprocessor 10.

[33] The user programs a corresponding RAM control signal so that the CL of the RAM 20 stored in the memory control table of the microprocessor 10 corresponds to one clock period of the microprocessor 10 and programs a corresponding RAM control signal so that a CAS/ signal of the RAM 20 is maintained in a low output state, that is, the CAS/ signal is enabled only for a 1/4 clock of the microprocessor 10.

[34] In order to activate the clock suspension function to maintain the data outputting of the RAM for two clock periods (one clock period of the microprocessor 10), the user programs a corresponding RAM control signal so that the clock enable signal CKE is maintained in the low state for a 1/4 clock period of the microprocessor 10.

[35] The user programs so that when the clock enable signal CKE is enabled, the microprocessor 10 can read a data from the RAM 20 at a rising edge of the next clock. The user programs such that an RP of the RAM 20 existing in the memory control table of the microprocessor 10 corresponds to one clock period of the microprocessor 10 (which is equivalent to two clock periods of the RAM 20), so that when one data is drawn out from the RAM 20, the RAM 20 can be precharged.

[36] The microprocessor 10 reads a data from the RAM 20 while a clock synchronization is being made between the microprocessor 10 and the RAM 20 will now be described. The memory controller of the microprocessor 10 simultaneously outputs RAM control signals to enable the CS/ signal (a signal for selecting a memory cell) and the RAS/ signal (a row address strobe signal). The CS/ signal and the RAS/ signal of the RAM 20 are simultaneously enabled by the RAM control signals.

[37] At this time, the low state of the CS/ signal and the RAS/ signal, that is, the CS/ signal and the RAS/ signal are enabled, is maintained only for the 1/4 clock of the microprocessor 10 ((1), (2)).

[38] Since the RCD has been programmed to correspond to one clock period of the microprocessor 10, when one clock period of the microprocessor 10 elapses from a point that the RAS/ signal is enabled, the memory controller outputs a RAM control signal to enable the CAS/ signal (column address strobe signal).

[39] The CAS/ signal of the RAM 20 is enabled by the outputted RAM control signal, and the enabled state of the CAS/ signal is maintained for the 1/4 clock period of the microprocessor 10. At this time, the CL is equivalent to one clock period of the microprocessor 10.

[40] When the CAS/ signal is enabled, the microprocessor 10 outputs a RAM control signal to enable the CKE signal and the CKE signal of the RAM 20 is enabled according to the RAM control signal (the CKE signal is maintained in the enabled state for the 1/4 clock period of the microprocessor 10).

[41] While the data (D0) output of the RAM 20 is maintained for the two clock periods of the RAM 20 according to the enabled CKE signal, the microprocessor 10 samples a data D0 at a rising edge (point 'A') of the next clock (the next clock of the microprocessor 10) ((5), (6)).

[42] When one data (D0) is outputted, a RAM control signal for precharge of the RAM 20 is outputted from the microprocessor 10, and at this time, the RP of the RAM 20 is given as long as one clock period of the microprocessor 10 ((7), (8)). When one read period

is finished in this manner, a new read period starts (9), of which operations are the same as described above.

[43] Figure 6 illustrates an exemplary timing diagram showing a clock-synchronizing method for a burst write operation of the microprocessor in accordance with still another embodiment of the present invention.

[44] If the RAM 20 has two clock periods of 100MHz (the operation clock of the microprocessor 10) as an operation latency in operation of a data outputting, an RCD (RAS to CAS Delay), a CL (CAS Latency) and an RP (Precharge time) of the RAM 20 are respectively two clock periods of 50 MHz of the RAM 20 which corresponds to one clock period of the operation clock of the microprocessor 10.

[45] The user programs RAM control signals in the following manner. That is, the user programs corresponding control signals so that RCD, CL and RP of the RAM 20 stored in the memory control table (UPM table) of the microprocessor 10 corresponds to one clock period of the microprocessor 10.

[46] In addition, an RAS/ signal enabled during the RCD interval is programmed to be in an enabled state only for a 1/4 clock of the microprocessor 10. A CAS/ signal and a CKE signal enabled during the CL interval are programmed to be maintained in the enabled state only for the 1/4 clock of the microprocessor 10.

[47] The CKE signal is programmed by the user such that it is enabled at a rising edge of each clock of the microprocessor 10 until one period of the burst write is completed, and the enabled state is maintained only for the 1/4 clock of the microprocessor 10.

[48] An operation that the microprocessor 10 burst-writes a data to the RAM 20 while a clock synchronization is being made between the microprocessor 10 and the RAM 20 will now be described.

[49] The memory controller of the microprocessor 10 simultaneously outputs RAM control signals to enable the CS/ signal and the RAS/ signal. As the CS/ signal and the RAS/ signal of the RAM 20 are simultaneously enabled by the RAM control signals, the RAM 20 samples a row address. At this time, the enabled state (that is, a low state) of the CS/ signal and the RAS/ signal are maintained only for a 1/4 clock of the microprocessor 10 ((1), (2)).

[50] Since the RCD has been programmed to correspond to one clock period of the microprocessor 10, when one clock period of the microprocessor 10 elapses from a point when the RAS/ signal is enabled, the memory controller simultaneously outputs a RAM control signal to enable the CAS/ signal and a RAM control signal to enable the CKE signal.

[51] When the CAS/ signal and the CKE signal of the RAM 20 are enabled by the simultaneously outputted RAM control signals (the enabled state of the CAS/ signal and the enabled state of the CKE signal0 are maintained for the 1/4 clock period of the microprocessor 10), the RAM 20 samples a column address at a point 'B' and at the same time samples a data (D0) from the microprocessor 10 and writes it in a corresponding region ((3), (4)).

[52] The RAM 20 performs a data sampling at a current clock (the point 'B') by the enabled CKE signal and does not perform a data sampling in the next clock. Thus, the RAM

20 reads a data for two clock periods of the RAM (for one clock period of the microprocessor). The microprocessor 10 enables the CKE signal of the RAM 20 at the rising edge of each clock of the microprocessor 10 until one period of the burst write is completed. As a matter of course, the low state of the enabled CKE signal is maintained for the 1/4 clock of the microprocessor 10. Since the CKE signal is enabled for each clock of the microprocessor 10 for one period of the burst write, the RAM 20 samples data (D1-D3) at the rising edge of each clock of the microprocessor 10 according to the clock suspension function ((5)-(9)).

[53] When one period of the burst write is completed, the RAM 20 is precharged (not shown in Figure 6). At this time, the CL can be one clock period of the microprocessor 10. In this manner, the microprocessor 10 can generate a RAM control signal at a doubled clock speed of the operation clock of the microprocessor 10, each of the reading and writing timing of the RAM 20 can be delayed by one clock period of the RAM 20, and the RAM 20 has the same operation latency as one clock period of the microprocessor 10. Therefore, the microprocessor 10 and the RAM 20 each having a different clock can be mutually interfaced while using their own clock as it is.

[54] Figure 7 is a table showing comparison results between a performance of a related art interfacing method and that of an interfacing method in accordance with one embodiment of the present invention. It is noted from Figure 7 that the interfacing method of the present invention has an improved performance from a minimum 25% to a maximum 100% compared to the interfacing method of the related art.

[55] The present invention is adoptable to interfacing for a mode register set for setting a mode of a RAM, for a refresh command for refreshing the RAM, or the like, as well as the interfacing for reading/writing of data between the microprocessor and the RAM.

[56] As so far described, the clock-synchronizing apparatus and method of devices with a different clock of the present invention has the following advantages. That is, since devices with a different clock speed can interface with each other by using their own clock as it is, it is not necessary to lower a clock of a device with a fast clock speed down to be the same as a slow clock of the opposite clock, a performance degradation of the device with the fast clock speed can be minimized.

[57] In addition, since the device with the fast clock speed can interface by using its own clock as it is, an access latency that a device with a slow clock speed accesses a device with the fast clock speed can be reduced and a transmission band with between the two devices can be effectively used.

[58] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structure described herein as performing the recited function and not only structural equivalents but also equivalent structures.